REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 1, 3, 5-11, 13, 15-21, 23-35, 37-44, and 46-52 are pending, wherein claims 1, 3, 5-11, 13, 15-21, 25-34, 37-44, 51 and 52 are currently amended, Claims 23-24, 35, 37 and 46-50 are withdrawn and currently amended, Claims 51 and 52 are newly added and Claims 2, 4, 12, 14, 22, 36 and 45 are canceled.

Response to Election/Restrictions

The Examiner has the opinion that "amended claims 23-24, 35, 37 and 46-50 were withdrawn from consideration because they are not supported by the elected species; note that in figure 2 does not show "a third portion" (emphasis added); note that the elected species includes only two portions one for a solder bump connection and a second one for testing or wire bonding."

Applicants respectfully traverse the Examiner's opinion. Claims 23-24, 35, 37 and 46-50 are supported in FIG. 2d within species 4 (figs. 1d and 2d) applicants elected in the reply filed on Sep. 7, 2005. In FIG. 2d, there are three portions 152, 154 and 158; one portion 152 is used to have a bump 160 formed thereover; another one portion 154 is used to be in contact with a testing probe; the other one portion 158 is used to be wirebonded thereto. Therefore, it is believed that Claims 23-24, 35, 37 and 46-50 should be examined because Caims 23-24, 35, 37 and 46-50 are supported in species 4, especially in FIG. 2d.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 1, 3, 5-11, 13, 15-21 and 23-26:

As currently amended, independent claim 1 is recited below:

"1. A circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises a first portion used to have a bump formed thereover and a second portion comprising a gold layer, wherein said gold layer is used to be in contact with a testing probe, and wherein said first portion is connected to said second portion."

Reconsideration of Claims 1, 4, 5, 8-11, 13, 17-20, 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. (US6,287,893) in view of Kim (US5,854,513), of Claims 2 and 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. (US6,287,893) in view of Kim (US5,854,513) further in view of Sato et al. (US4,051,508), of Claims 6 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. in view of Kim further in view of Lee (US20040036170), of Claims 15 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. in view of Kim further in view of Kitayama et al. (US5,646,439), and of Claim 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. in view of Kim

further in view of Harper is requested based on the following remarks.

In merits to meet requirement of patentability, Applicants have amended Claim 1 with adding the limitation that "said patterned circuit layer comprises a second portion comprising a gold layer, wherein said gold layer is used to be in contact with a testing probe, and wherein said first portion is connected to said second portion."

Applicants respectfully assert that the circuit component claimed in claim 1 patentably distinguishes over Elenius et al. (US6,287,893) in view of Kim (US5,854,513).

Elenius et al. teach a circuit component comprising a semiconductor substrate 14, a conductive bond pad 18 over the semiconductor substrate 14 and a passivation layer 22. An opening in the passivation layer 22 exposes a top surface of the bond pad 18. The circuit component further comprises a patterned circuit layer 30 connected to the top surface of the bond pad 18, wherein the patterned circuit layer 30 comprises a portion used to have a bump formed thereover (*See FIG. 2*). However, Elenius et al. fail to teach, hint or suggest the patterned circuit layer 30 may comprise another portion used to be in contact with a testing probe.

Kim teaches that a circuit component comprises a patterned circuit layer 22 and 23 comprising a first portion used to have a bump 27 formed thereover and a second portion used to be in contact with a testing probe. The patterned circuit layer 22 and 23 is under a passivation layer 24, multiple openings in the passivation layer 24 exposing the first and second portions of the patterned circuit layer 22 and 23 (*See FIG. 3*).

As mentioned above, Elenius et al. fail to teach how the circuit component can be in contact with a testing probe when Elenius et al. face a bump 28 to be formed on a patterned circuit layer 30 connected to a top surface of a metallization structure 18

exposed by an opening in a passivation layer 22. Even under the teaching by Elenius et al. in view of Kim, only the subject matter that "during a testing step, the pad 18 exposed by an opening in the passivation layer 12 can be in contact with a testing probe" can be anticipated, because Kim only teaches, during a testing step, a pad exposed by an opening in the passivation layer 24 is in contact with a testing probe (*See FIG. 3*). After the testing step, the patterned circuit layer 30 is formed over the passivation layer 12. No one teaches a patterned circuit layer over a passivation layer may have a portion used to be in contact with a testing probe.

Furthermore, both Elenius et al. and Kim fail to teach a patterned circuit layer may have a gold layer used to be in contact with a testing probe, as currently claimed in claim 1. The gold layer has an advantage, such as not to be easily damaged by chemicals used in the subsequent processes for forming bumps, which is not anticipated by Elenius et al. and Kim. Even Sato et al. (US4,051,508) teach a trace comprises a gold layer 4 having a thickness of greater than 2 microns (*See 2B and col. 3, lines 34-37*), but Sato et al. fail to teach the gold layer may be used to be in contact with a testing probe, as claimed in claim 1.

As a result, the subject matters as a whole claimed in claim 1 can not be attained. Withdrawal of claim 1 under 35 U.S.C. 103(a) is respectfully requested.

In response to the rejection for Claim 13, both Elenius et al. and Kim fail to teach a patterned circuit layer over a passivation layer may comprises a metal line connecting a first portion used to have a bump formed thereover and a second portion used to be in contact with a testing probe.

In response to the rejection for Claim 21, the Examiner failed to provide the document number for Harper. Showing the document number for Harper is respectfully

requested.

In response to the rejection for Claims 25 and 26, Applicants consider paragraph [0028] of current specification does support the criticality. The paragraph [0028] of current specification disclosed that "During testing, a testing probe can contact the testing pad, for testing the chip structure without contacting the bump". The Examiner admitted the "pitches" are subject to optimization. For the purpose of "optimization", the pitch should be long enough so that the testing probe does not contact the bump during the testing. On the contrary, the current invention is designed to have a short pitch and still the "no contact between the testing probe and the bump". No one teaches how long can be the pitch between the portion used to have a bump formed thereover and the portion used to be in contact with a testing probe.

For at least the foregoing reasons, applicants respectfully submit independent claim 1 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 3, 5-11, 13, 15-21 and 23-26 patently define over the prior art as well.

Response to Claims 27-35, 37-44, 51 and 52:

As currently amended, independent claim 27 is recited below:

"27. A circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening,

wherein said patterned circuit layer comprises a first portion used to have a bump formed thereover and a second portion comprising a copper layer, wherein said copper layer is used to be wirebonded thereover."

Reconsideration of Claims 27-29, 32-34, 40-42 and 44 rejected under 35 U.S.C. 103(a) as being unpatentable over Lam et al. (US6,511,901) in view of Liao et al. (US6,590,295), of Claims 30, 31 and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Lam et al. in view of in view of Liao et al. further in view of Elenius et al. (US6,287,893), of Claims 38 and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Lam et al. in view of Liao et al. further in view of Kitayama et al. (US5,646,439), and of Claim 43 rejected under 35 U.S.C. 103(a) as being unpatentable over Lam et al. in view of Liao et al. further in view of Kim (US5,854,513) further in view of Harper is requested based on the following remarks.

In merits to meet requirement of patentability, Applicants have amended Claim 27 with adding the limitation that "said patterned circuit layer comprises a second portion comprising a copper layer, wherein said copper layer is used to be wirebonded thereover."

Applicants respectfully assert that the circuit component claimed in claim 27 patentably distinguishes over Lam et al. (US6,511,901) and Liao et al. (US6,590,295).

Lam et al. teach a circuit component comprising a semiconductor substrate 104, a bond pad 102 over the semiconductor substrate 104 and a passivation layer 202. An opening in the passivation layer 202 exposes a top surface of the bond pad 102. The circuit component further comprises a patterned circuit layer 204, 206 and 208 connected to the top surface of the bond pad 102, wherein the patterned circuit layer 204, 206 and 208 comprises a first portion used to have a bump formed thereover and a second portion

used to be wirebonded thereto (*See FIG. 2I*).

Lam et al. teach that a portion of the copper layer 208 and the nickel layer 206 is removed for forming an opening in the copper layer 208 exposing the aluminum layer 202 used to be wirebonded thereto (*See FIG. 2I and col. 3, lines 49-61*) because Lam et al. consider that "Recalling further that due to its high oxidation rate, copper is less than ideal for wire bonding applications, whereas aluminum is a bondable metal", extracted from col. 3, lines 49-51. Under Lam et al.'s teaching, Applicants do not consider that the subject matter that "the copper layer 208 can be wirebonded thereover", as currently claimed in Claim 27, can be anticipated.

Liao et al. teach that a circuit component comprises a semiconductor substrate 12; a metallization structure 14 over said semiconductor substrate 12; a passivation layer 16 over said metallization structure 14, wherein an opening in said passivation layer 16 exposes a top surface of said metallization structure 14; and a patterned circuit layer 20 connected to said top surface, wherein said patterned circuit layer 20 comprises a copper layer, and wherein said patterned circuit layer 20 comprises a first portion used to have a bump 26 formed thereover (*See FIG. 3 and col. 9, lines 45-47*).

Liao et al. fail to teach, hint or suggest the copper layer can be used to be wirebonded thereover. Therefore, under the teaching by Lam et al. in view of Liao et al., Applicants do not consider that the subject matter that "the copper layer 208, referred to by Lam et al., can be wirebonded thereover", as claimed in Claim 27, can be anticipated.

As a result, the subject matters as a whole claimed in claim 27 can not be attained. Withdrawal of claim 27 under 35 U.S.C. 103(a) is respectfully requested.

In response to the rejection for Claim 43, the Examiner failed to provide the

document number for Harper. Showing the document number for Harper is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 27 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 28-35, 37-44, 51 and 52 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

Sincerely yours,

Winston Hsu Date: 11/06/2006

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)